## SHIVAKAR DUTT VERMA

India | P: +91 7318365789 | Email: [shivakarduttverma176@gmail.com](mailto:shivakarduttverma176@gmail.com)

LinkedIn: www.linkedin.com/in/shivakar-dutt-verma

**PROFILE SUMMARY**

Aspiring **VLSI Layout Engineer** with a solid academic foundation in Electronics and Communication Engineering and hands-on experience in full-custom and semi-custom layout design using industry-standard EDA tools. Skilled in physical design concepts such as DRC, LVS, and LPE, with practical exposure to CMOS technology, parasitic analysis, and Verilog-based circuit implementation.

**EDUCATION**

**Veer Bahadur Singh Purvanchal University** — Jaunpur, U.P., India

**Bachelor of Technology (B.Tech)** | Electronic & Communication Engineering *2020–2024* | Percentage: 68.32%

**TRAINING & EXPERIENCE**

**Trainee - Fundamentals of VLSI Design  
 VLSI Expert Pvt. Ltd.**, Noida, U.P., India | July 2024 – Present

* **Linux Fundamental & Scripting**: Overview of Linux operating system architecture, basic commands, shell scripting, file system navigation, environment and path variable management, and efficient text editing using vi/vim editor.
* **Layout Design:** Designed stick diagrams and layouts with folding and fingering techniques for area optimization. Prevented latch-up in CMOS circuits. Worked on full-custom and semi-custom design methodologies.
* **Parasitic Extraction & Verification:** Conducted Layout vs. Schematic (LVS), Design Rule Check (DRC), and Layout Parasitic Extraction (LPE) using industry-standard tools.
* **CMOS Design:** Understanding ofMOSFET operation principles, CMOS fabrication processes, threshold voltage considerations, and scaling challenges in modern semiconductor technology.
* **Digital Electronics:** Designed and analyzed logic gates, flip-flops, counters, multiplexers, and other combinational/sequential circuits.
* **Verilog HDL & Digital Modeling:** Structured modeling at gate-level, dataflow, and behavioral abstraction levels, Finite State Machine (FSM) design including Moore and Mealy models, switch-level transistor modeling, and comprehensive test bench development for functional and timing verification.
* **RTL Design & Verification:** Developed and simulated various combinational and sequential logic modules using Verilog HDL.
* **Logic Synthesis:** Conversion of RTL code to gate-level netlists using standard cell libraries.
* **EDA Tools Used:** Cadence Virtuoso, Synopsys Custom Compiler, Design Compiler, Verdi

**PROJECTS**

**Design & Implementation of 4-Bit Arithmetic Logical Unit (ALU) using CMOS Technology**

* Designed basic **CMOS** logic gates such as **AND, OR, XOR**, and components like **Multiplexers** and **Full Adders**
* Developed **1-bit** and **4-bit ALU**, complete with block diagrams and schematic verification through truth tables
* Performed performance evaluation based on complexity, **Delay**, and **Power Consumption** under various input conditions through simulation experiments
* Gained hands-on experience with industry-standard tools such as **Cadence Virtuoso**

**Design & Implementation of 1-Bit ALU & Full Adder (4-bit, 8-bit & 32-bit) using CMOS and Standard Cell Technology**

* Designed schematic and physical **layout** for 1-bit ALU and Full Adders (4-bit, 8-bit, and 32-bit) using both CMOS transistor-level design and standard cell libraries
* Performed **DRC (Design Rule Check)** and **LVS (Layout vs. Schematic)** verification to ensure correctness and manufacturability of layouts.
* Performed layout and post-layout verification using **Synopsys Custom Compiler** and analyzed simulation waveforms.

**Design & Implementation of NAND and NOR Logic gate using CMOS Technology**

* Designed **schematic and physical layouts** for NAND and NOR gates using CMOS transistor-level design methodology.
* Applied **fingering and folding techniques** to optimize transistor sizing, reduce parasitic effects, and minimize layout area while maintaining performance.
* Performed **DRC (Design Rule Check)** and **LVS (Layout vs. Schematic)** verification to ensure correctness and manufacturability of layouts.
* Gained practical experience with **SYNOPSYS** **Custom Compiler** and standard industry practices in **full-custom VLSI design**.

**TECHNICAL SKILLS**

* **EDA Tools**: ***Synopsys:*** HSpice (Circuit Simulation), IC Compiler (Place & Route), IC Validator (Physical Verification), Design Compiler (Logic Synthesis), StarRC (Parasitic Extraction), SPYGLASS, Custom Compiler (Layout Design), Verdi (RTL Debugging & Waveform Analysis), ***Cadence:*** Virtuoso (Schematic/Layout Design)
* **Programming & Scripting Languages**: Verilog HDL (RTL Design & Verification), C Programming, TCL, Shell Scripting, Linux
* **Design & Simulation**: Full-Custom & Semi-Custom Layout Design, Design Rule Check (DRC), Layout vs. Schematic (LVS), Layout Parasitic Extraction (LPE), Standard Cell-Based Design, Physical Verification, Gate-Level Simulation

**CERTIFICATIONS & TRAINING**

* Certificate in Computer Concepts — NIELIT, May 2019
* VLSI Design using Cadence (Two-Week Online Training Program) — NIELIT